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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/614,154	07/11/2000	Martin J. Edwards	PHB 34,365	1602
24737	7590	10/30/2003	EXAMINER	
PHILIPS INTELLECTUAL PROPERTY & STANDARDS			SHAPIRO, LEONID	
P.O. BOX 3001			ART UNIT	PAPER NUMBER
BRIARCLIFF MANOR, NY 10510			2673	14
DATE MAILED: 10/30/2003				

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)	
	09/614,154	EDWARDS, MARTIN J.	
	Examiner	Art Unit	
	Leonid Shapiro	2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1) Responsive to communication(s) filed on 04 September 2003.

2a) This action is FINAL.                    2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4) Claim(s) 9-12 is/are pending in the application.

4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

5) Claim(s) \_\_\_\_\_ is/are allowed.

6) Claim(s) 9-12 is/are rejected.

7) Claim(s) \_\_\_\_\_ is/are objected to.

8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on 04 September 2003 is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) The proposed drawing correction filed on \_\_\_\_\_ is: a) approved b) disapproved by the Examiner.  
If approved, corrected drawings are required in reply to this Office action.

12) The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) All b) Some \* c) None of:  
1. Certified copies of the priority documents have been received.  
2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.

14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).  
a) The translation of the foreign language provisional application has been received.

15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____ .
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .	6) <input type="checkbox"/> Other: _____ .

***Drawings***

1. The corrected drawings were received and approved on 04-01-03. These drawing sheets are 1/3 and 2/3 including Figs. 1-3.



***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 9-10 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsueda et al. (US Patent 6,384,806 B1) in view of Enami et al. (US Patent no. 5,892,493).

As to claim 9, Matsueda et al. teaches an active matrix array device comprising: substrate; an array of individually addressable matrix elements carried on substrate, a set of address conductors connected to array of matrix elements and carried on substrate, set of address conductors being arranged in a series of groups with each group including successive address conductors (See Fig. 15-17, items 10, 100, 200, 41, 42, 30, in description See Col.20, Lines 30-64 and Col.19, lines 13-58) and an addressing circuit including a multiplexing circuit (inside of 200A and 200B, Fig. 17) integrated on substrate and connected to set of conductors, multiplexing circuit having a plurality of signal bus lines, multiplexing circuit being arranged to couple sequentially each group of set of address conductors to plurality of signal lines with each address conductor in a group being coupled to a respective one of signal bus lines (inside of 200A and 200B, Fig. 17) and a plurality of signal processing circuits (digital drive circuit 200 of

Fig. 15) integrated on substrate, each signal processing circuit connected to a respective bus line (See Fig. 15-17, items 10, 100, 101, 200, 41, 42, 30, in description See Col.20, Lines 30-64 and Col.19, lines 13-58).

Matsueda et al. does not show a first signal processing circuit associated with a first address conductor of a first group of address conductor and a second signal processing circuit associated with a last address conductor of a second group of address conductors are adjacent on substrate.

Enami et al. teaches a first signal processing circuit (inside of multiplexer 38) associated with a first address conductor of a first group of address conductor and a second signal processing circuit (inside of multiplexer 38) associated with a last address conductor of a second group of address conductors are adjacent on substrate (See Fig. 1, items dnA, d1B, in description See Col. 7, Lines 46-61).

It would have been obvious to one of ordinary skill in the art at the time of invention to implement a first signal processing circuit associated with a first address conductor of a first group of address conductor and a second signal processing circuit associated with a last address conductor of a second group of address conductors are adjacent on substrate as shown by Enami et al. in the Matsueda et al. apparatus in order to selectively connect the driver to any one of sets data line groups (See Col. 2, Lines 8-15 in the Enami et al. reference).

As to claim 10, Matsueda et al. teaches signal processing circuits are arranged in series in a line parallel to multiplexing circuit (See Figs. 15-17, items 200, 101A, 101B, 200A, 200B, in description See Col. 19, Lines 28-34 and Col.20, Lines 29-48). Notice that multiplexing circuits are in the shift registers on both sides of LCD panel.

As to claim 12, Matsueda et al. teaches an active matrix array device with order in which processing circuit blocks are arranged physically on the device substrate is different to the physical order of the signal bus lines to which they are respectively connected (See Fig. 17, items 200A, 200B, in description See Col.20, Lines 29-45). Notice that D/A converters on both sides of LCD panel.

3. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Matsueda et al. and Enami et al. as applied to claim 9 above, and further in view of Yamazaki et al. (US Patent 6, 144,426).

Matsueda et al. and Enami et al. do not show a first subset of signal processing circuits are arranged in a first row and a second subset of signal processing circuits are arranged in a second row and offset from the first row in a brick-like fashion.

Yamazaki et al. teaches place microlens array in brick fashion (arranged like laid bricks) (See Fig. 3, item 105, in description see Col. 8, Lines 9-18).

It would have been obvious to one of ordinary skill in the art at the time of invention to implement layout of signal processing circuits in a brick-like fashion as shown by Yamazaki et al. in the Matsueda et al. and Enami et al. apparatus in order to selectively connect the driver to any one of sets data line groups (See Col. 2, Lines 8-15 in the Enami et al. reference).

#### *Response to Amendment*

4. Applicant's arguments filed on 06-10-03 with respect to claims 9-12 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

The Lee et al. (US Patent No. 5,510,807) reference discloses data driver circuit and associated method for use with scanned LCD Video Display.

The DaCosta et al. (US Patent No. 6,281,891 B1) reference discloses display with array And multiplexer on substrate and with attached digital-to-analog converter integrated circuit having many outputs.

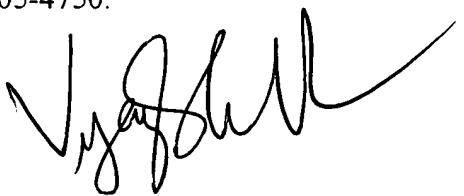
***Telephone inquire***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonid Shapiro whose telephone number is 703-305-5661. The examiner can normally be reached on 8 a.m. to 5 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 703-305-4938. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-4750.

ls



VIJAY SHANKAR  
PRIMARY EXAMINER